

# Notice of Allowability

Application No.

09/493,270

Examiner

Abbas I Abdulsalam

Applicant(s)

SHIGETA, KAZUYUKI

Art Unit

2674

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to 07/02/2004.
2. ☒ The allowed claim(s) is/are 1-9 and 33-39 (renumbered as claims 1-16).
3. ☒ The drawings filed on 28 January 2000 are accepted by the Examiner.
4. ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
  - a) ☒ All    b) ☐ Some\*    c) ☐ None    of the:
    1. ☒ Certified copies of the priority documents have been received.
    2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
    3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

\* Certified copies not received: \_\_\_\_\_.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.  
**THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.**

5. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.
  6. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
    - (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      - 1) ☐ hereto or 2) ☐ to Paper No./Mail Date \_\_\_\_\_.
    - (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date \_\_\_\_\_.
- Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).
7. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

## Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3. ☐ Information Disclosure Statements (PTO-1449 or PTO/SB/08), Paper No./Mail Date \_\_\_\_\_
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application (PTO-152)
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date \_\_\_\_\_
7. ☐ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other \_\_\_\_\_

  
**XIAO WU**  
**PRIMARY EXAMINER**

## **DETAILED ACTION**

### ***Allowable Subject Matter***

1. The following is an examiner's statement of reasons for allowance:

Satoh et al. (USPN 6789210) teach a data processor comprising: a bus control circuit adapted to be interfaced with a synchronous DRAM which can be accessed in synchronism with a clock signal; Satoh et al. disclose a plurality of data processing modules coupled to the bus control circuit for producing data and addresses for accessing a memory; and a clock driver for feeding intrinsic operation clocks to the data processing modules and for feeding the clock signal for accessing the memory in synchronism with the operations of said data processing modules to be operated by the operation clock signals, to the outside (See the abstract).

Regarding claim 1, none of the cited prior art teaches or suggests an image processing device comprising a memory unit having a memory region for storing images of at least one screen, a memory control unit for performing an input system operation to write image data to the memory unit by using a first clock and a first image synchronizing signal and for performing an output system operation to output image data read out from the memory unit by using a second clock and a second image synchronizing signal, a clock generating unit for generating the second clock, and a synchronizing control unit for inputting the second clock and for outputting the second image synchronizing signal, wherein said synchronizing control unit generates a third image synchronizing signal asynchronous to the first image synchronizing signal by dividing the second clock and a fourth image synchronizing signal, and being synchronized to the first image synchronizing signal by using the second clock and selects one of the third image synchronizing

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signal and the fourth image synchronizing signal to output it as the second image synchronizing signal.

Regarding claim 4 (renumbered as claim 11), none of the cited prior art teaches or suggests an image processing device, comprising a memory unit having a region for storing images of at least one screen, a memory control unit for performing an input system operation to write image data to the memory unit on by using a plurality of first clocks and a plurality of first image synchronizing signals synchronized to a plurality of input signals inputted to said plurality of input system signal processing units and for performing an output system operation to output image data read out from the memory unit by using a second clock and a second image synchronizing signal, a clock generating unit for generating the second clock, and a synchronizing control unit for inputting the second clock and for outputting the second image synchronizing signal. Wherein said synchronizing control unit generates a third image synchronizing signal asynchronous to the first image synchronizing signals by dividing the second clock and the fourth image synchronizing signals, and being synchronized to the first image synchronizing signals by using the second clock and selects one of the third image synchronizing signal and the fourth image synchronizing signals to output it as the second image synchronizing signal.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

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2. Any inquiry concerning this communication or earlier communication from the examiner should be directed to **Abbas Abdulsalam** whose telephone number is **(703) 305-8591**. The examiner can normally be reached on Monday through Friday (9:00-5:30).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, **Richard Hjerpe**, can be reached at **(703) 305-4709**.

**Any response to this action should be mailed to:**

Commissioner of patents and Trademarks

Washington, D.C. 20231

**or faxed to:**

**(703) 872-9314**

Hand delivered responses should be brought to Crystal Park II, Crystal Drive, Arlington, VA, Sixth Floor (Receptionist).

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Technology center 2600 customer Service office whose telephone number is (703) 306-0377.

Abbas Abdulsalam

Examiner

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September 8, 2004

  
**XIAO WU**  
**PRIMARY EXAMINER**